Efficient Synthesis of Reversible Circuits Using Quantum Dot Cellular Automata

---

SUBMITTED TO : Dr Ramesh Kumar V
SUBMITTED BY :
ALKESH SHUKLA (S20210020252)
Anish Kamble (S20210020253)

Abstract: Quantum-dot cellular automata (QCA) offer a promising nanoscale computing technology, capitalizing on quantum mechanical electron tunneling and electrostatic interactions between adjacent quantum dots. QCA exhibits potential advantages such as higher speed, lower power consumption, and a reduced physical footprint compared to traditional complementary metal-oxide semiconductor (CMOS) technology. Notably, heat dissipation remains a pressing concern in modern electronic device design, primarily attributed to bit loss. To mitigate this issue, reversible circuits have emerged as a viable solution. This study evaluates the efficacy of reversible computing in QCA, with a particular focus on CNOT and TOFFOLI gates. As QCA designs evolve, a significant reduction in cell size, time delay, circuit area, and the use of majority gates becomes evident. Furthermore, this research expands the scope of reversible circuits by introducing additional components, including the reversible XOR gate, half adder, half subtractor, 2-to-1 multiplexer, 4-to-1 multiplexer, reversible arithmetic unit (AU), reversible logic unit (LU), and reversible arithmetic logic unit (ALU). This extension contributes to the ongoing advancement of reversible computing within the QCA framework.

INDEX TERMS: Quantum-dot cellular automata, Reversible gates, CNOT gate, TOFFOLI gate, SWAP Circuit, CNOT Gate, TOFFOLI Gate, Electron Tunnelling, Quantum Dots, Reversible Logic Gates, XOR Gate, Half Adder, Half Subtractor, Multiplexer, Arithmetic Unit (AU), Logic Unit (LU), Arithmetic Logic Unit (ALU).

Introduction :

In the ever-evolving landscape of electronic devices and computing technologies, quantum-dot cellular automata (QCA) has emerged as a promising nanoscale computing solution. Leveraging quantum mechanical electron tunnelling and electrostatic interactions among adjacent quantum dots, QCA offers a potential paradigm shift. It boasts the allure of higher computational speeds, lower power consumption, and a notably reduced physical footprint when compared to the

conventional framework of complementary metal-oxide semiconductor (CMOS) technology. However, amid these advancements, a persistent challenge looms large: the dissipation of heat in electronic devices. This challenge is intrinsically tied to the concept of bit loss, a phenomenon that poses significant hindrances to the efficiency and durability of electronic equipment. In response to this challenge, the research community has turned to the innovative approach of reversible circuits as a viable solution. Reversible computing has proven to be a compelling strategy to address the issue of heat dissipation. This study embarks on a comprehensive assessment of the efficacy of reversible computing within the realm of QCA, with a particular emphasis on the utilization of CNOT and TOFFOLI gates. As the designs of QCA continue to evolve, the findings of this research unveil a notable transformation in various critical parameters. These include a substantial reduction in cell size, diminished time delay, a more compact circuit area, and a decreased reliance on majority gates. Moreover, the scope of reversible circuits is expanded to encompass an array of essential components, including the reversible XOR gate, half adder, half subtractor, 2-to-1 multiplexer, 4-to-1 multiplexer, reversible Arithmetic Unit (AU), Logic Unit (LU), and Arithmetic Logic Unit (ALU). This extension contributes significantly to the perpetual advancement of reversible computing within the QCA framework. This research paper delves into the intersection of quantum-dot cellular automata, reversible computing, and the ongoing quest to overcome the formidable challenge of heat dissipation in modern electronic device design. It explores not only the theoretical underpinnings but also practical implementations that promise to shape the future of nanoscale computing.

QCA Basics

Ⅰ.Basics of quantum dot construction:

In general there are three statuses in the polarization of cells. Primary, secondary and tertiary status. Primary status in which electrons are not placed in any polarized manner. In secondary electrons are polarized positively and in tertiary electrons are polarized negatively.positive polarization denoted by (P=+1) and negative is denoted by (P= -1).

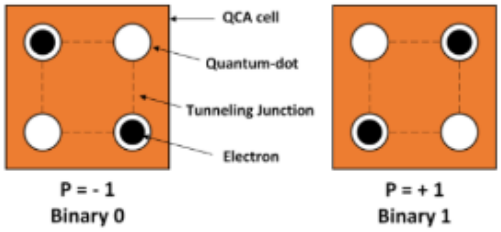


Figure 1. QCA cell polarization.

Below equation represents KINK energy or says about the polarization of cells.

$$E^{i,j} = \frac{1}{4\prod \varepsilon_0 \varepsilon_r} \sum_{n=1}^{4} \sum_{m=1}^{4} \frac{qn^i qm^i}{|rn^i - rm^i|}$$

EQUATION - I

In the above equation ε0 permittivity of free space, εr is dielectric constant, qn_i is charge in dot n of cell i, rn_i i is the position of the dot in cell i,$|rm_i - rm_i|$ is the distance between the cells

Kink energy is the Energy difference between two cells with opposite polarity or the same polarity. Where E is the energy, P□ is the polarization of the cells n and P□ is the polarization of the cell m.

$$Ekink^{n,m} = E^{n,m}_{Pn \neq Pm} - E^{n,m}_{Pn=Pm}$$

EQUATION - Ⅱ. **Kink energy**

P_i gives the measurement of the polarization of each cell. Where pi is the polarization state of the cell, P□ is the polarization state of the neighboring cell, γ is the tunneling energy of the electron within the cell.

$$P_i = \frac{\frac{Ekink^{i,j}}{2\gamma}\sum jP_j}{\sqrt{1 + \left(\frac{Ekink^{i,j}}{2\gamma}\sum jP_j\right)^2}}$$

EQUATION -Ⅲ

Ⅱ. Qca wires

QCA cells perform computation by interfacing coulombically with neighboring cells to influence each other's polarization. The binary signal propagates from left to right because of the coulombic interactions between cells.

FIGURE Ⅱ represents 90 degrees-oriented cells whereas in **FIGURE** Ⅲ the cells are in 45 degrees orientation.

For example, if we are having input cell-1 with polarization (p = -1) and the next cell-2 with (p = +1) polarization, then a binary " 0 " (due to the input cell being polarized to -1) will propagate down the length of the wire because of the coulombic interaction between cells.

The main advantage of 45 deg wire is that we will get both the transmitted signal and its complement value without using an external inverter circuit.

FIGURE Ⅱ **45-degrees cells**

FIGURE Ⅲ

Figure 4 and Figure 5 says about the planarity of the QCA wires, in fig 4 the wires are crossing in a single layer and in fig-5 the wires are in multilayer so it is called multilayer crossing. The information transfers throw 'via' in multilayer crossing.

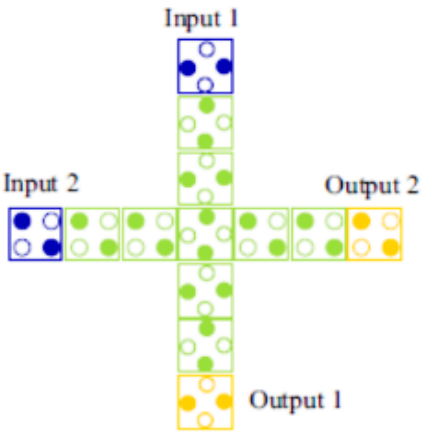


FIGURE Ⅳ. Coplanar Crossing

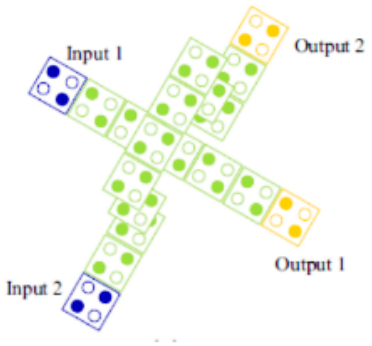


FIGURE Ⅴ. Multi-Layer Crossing

Ⅲ. Qca majority gate and inverter:

Majority Voting(MV) gate has 5 cells in total. The general output equation of the MV gate is xy+yz+zx, where x, y and z are inputs to the MV gate.MV gate is in the form of '+'.

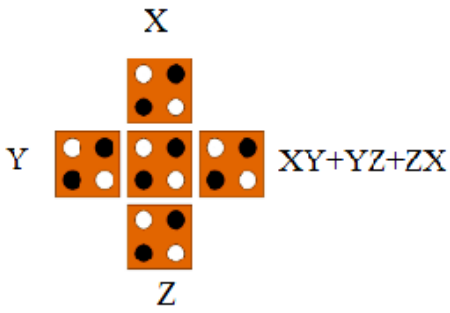


FIGURE Ⅵ. MV Gate

MV gate can also be used as AND gate and OR gate. This can be done by setting one of the input cells to a positive or negative polarization. Positive polarization gives OR gate functionality to the MV gate f(X, Y) = X+Y.

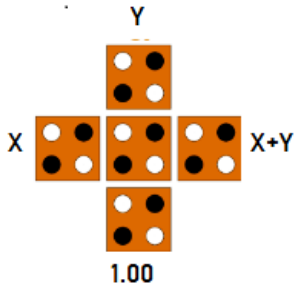


FIGURE Ⅶ. OR gate using MV gate

Negative polarization gives AND gate functionality to the MV gate f(X, Y) = X.Y.

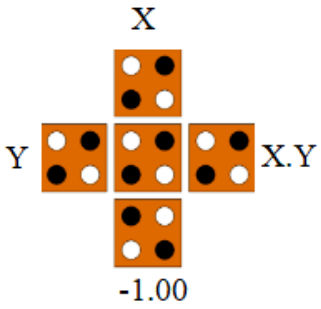


FIGURE Ⅷ. AND Gate using MV Gate

NOT Gates are also known as inverters.NOT gate inverts the inputs i.e, It converts 0 to 1 and vice versa. FIGURE Ⅸ and FIGURE Ⅹ are examples of NOT gates. FIGURE Ⅸ also called a ROBUST inverter because it has 2 ways to reach the output, chance of data loss is decreased due to multiple inputs. whereas FIGURE Ⅹ has only 1 way.

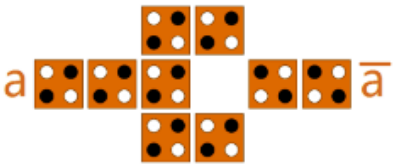


FIGURE Ⅸ. ROBUST inverter

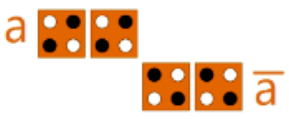


FIGURE X. Inverter

The functionality of the FIGURE X I QCA Design is NAND Gate. It is the combination of NOT gate and AND gate with negative polarization.

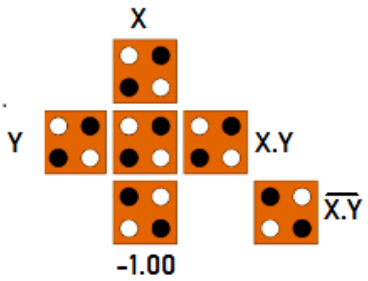


FIGURE X I. NOR Gate Using MV Gate

IV. Qca clocking

The clocking of QCA is achieved by measuring capacity barriers to the connected quantum dots. It controls the information flow and the synchronization in the circuit.

This clocking contains four phases 1)Switch 2)Hold 3)Release 4)Relax.

1) Switch phase: In this phase, the unpolarised electrons in cells are driven by some input and get polarized depending on their neighbor's polarization.

2) Hold: In this cells are held in some finite polarization either in high or low, simply a binary state.

3) Release: Here the given potential decreases gradually so that the cells lose their polarization slowly.

4) Relax: finally potential decreased completely hence cells remain in an unpolarised state or NULL state.

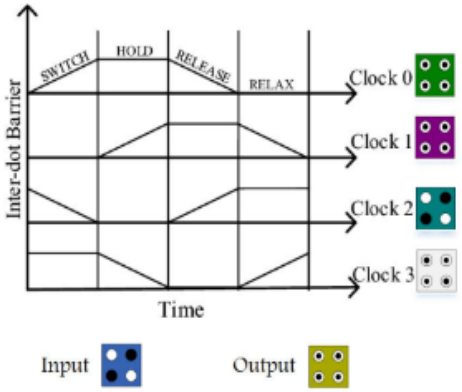


FIGURE X I I. Clock phases

V. Layout design rules

1) A single clock zone with the most cells possible: If the cells present in the same clock zone are maximum then it leads to maximum errors in the circuit. So to prevent this problem we use EQUATION-IV, which says about the number of cells to be present in the same clock zone.

$$N \leq \frac{E_k}{e^{kB}T}$$

EQUATION -IV

In this equation N represents the cell count in an array, T represents the operating temperature, and Ek represents the kink energy. As the number of cells is inversely proportional to the operating temperature, if the size of the cell decreases then the count of cells increases in the wire hence the operating temperature decreases as it is inversely proportional to T . If we run our circuit at higher temperatures the size of the cell decreases.

The data transferring speed decreases if the size of the wire is long and it will take more

time to propagate the signal from one input to another. To increase the data transfer speed we divided long wires into smaller ones with different clock zones.

2) A single clock zone with the fewest possible cells:

After dividing the large wire into smaller ones then each cell presents in its corresponding clock zone. If only one cell is present in one clock zone then there is a sudden change in direction of the signal that we are sending because of this sudden change errors will occur in results.

Therefore, we are limited to having a minimum of two cells in each clock zone in order to prevent this issue.

3) Possible Crossover:

As we have discussed earlier in the QCA WIRES section FIGURE Ⅳ and FIGURE Ⅴ represent coplanar and multilayer crossover.

In FIGURE IV, we correctly aligned both the 45 and 90-degree cells to avoid interference. A reliable operation of coplanar crossing is dependent on the temperature of the operation. As our main focus is on the condition of the wire, data transmission in the wire and power dissipation in QCA circuits.

We can choose the second type of crossover instead of coplanar crossover, it contains different layers on top of each other which reduces space and increases data transmission rate than coplanar circuits. We have advantages with multilayer crossover over coplanar but it is difficult to create multilayer wires.

So at present, we are bound to use coplanar crossover.

4) Timing design rules:

For instance, if two wires are connected in a coplanar crossover with inputs 1 and 2, practically both inputs must arrive at the junction simultaneously.

However, this won't happen in our reality circuit since the two wires are different lengths, therefore we must design the wires so that they are both in the same clocking zone and that there is a cell at the junction as well.

Temperature	1.000000
Cell Width(nm)	18.000000
Cell Height(nm)	18.000000
Relaxation Time	1.000000×10^(-15)
Time Step	1.000000×10^(-16)
Total Simulation Time	7.000000×10^(-11)
Clock High	9.800000×10^(-22)
Clock Low	3.800000×10^(-23)
Clock Shift	0.000000
Clock Amplitude Factor	2.000000
Radius of Effect	80.000000
Relative Permittivity	12.900000
Layer Separation	11.500000

REVERSIBLE LOGIC GATE:

The gates with the attribute of having an equal number of inputs and outputs are known as reversible gates or reversible logic gates. The amount of energy lost will be minimized when the number of inputs and outputs is equal.QCA Designer is used to simulate circuits and generate graphs of the outcomes. Different logic gates with various circuit layouts have been compared at various periods. We compared cell count, cell area, delay, MV gates, and wire crossover at the conclusion of each of the different gate circuits.

1] CNOT GATE

One qubit serves as the "control" and the other as the "target" in the controlled-NOT gate, also known as the controlled-x (CX) gate. Every time the control is in the state, it executes a NOT on the target. This gate induces entanglement in the case of a superposition of the control qubit.

The truth table of the CNOT gate. They are used to compare the output from the simulation for the verification of correctness.

Truth Table:

X	Y	A	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

TABLE 1: **CNOT Gate**

A) Feynman Gate - 2019

Feynman gate is proposed in the year 2019

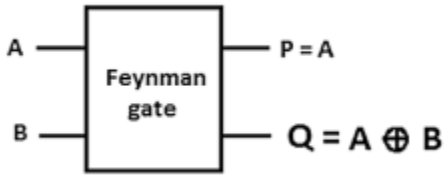


FIGURE 1(A) - Circuit representation of CNOT gate

The logical equation of the outputs are represented as

$$P = A$$
$$Q = A \hat{} B$$

In the logical expression ' ^ ' is referred to as XOR.

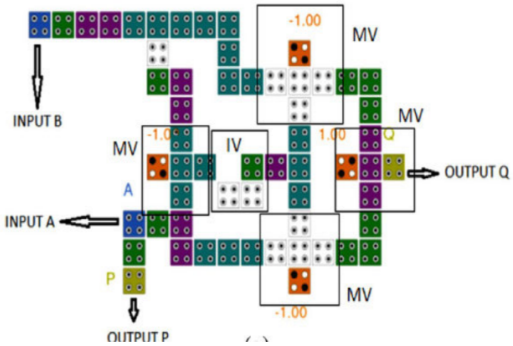


FIGURE 1(A) Feynman - 2019

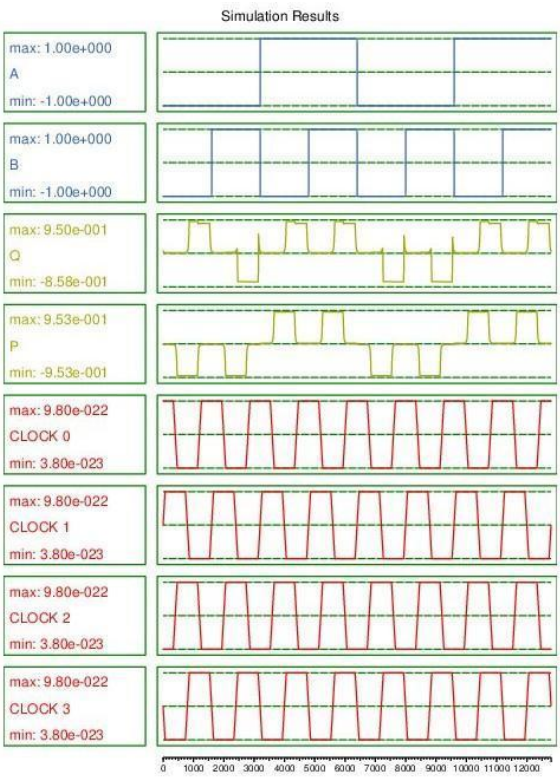


FIGURE1(A) - Feynman - 2019 Simulation

B) Feynman Gate - 2018

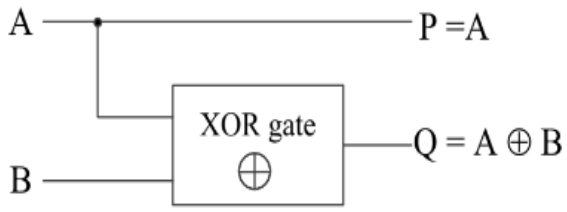


FIGURE 1(B) - Circuit representation of CNOT gate

For the circuit representation of CNOT Gate, A and B are inputs, P and Q are the Outputs. The logical equation of the outputs is represented as

P =A

Q = A^B

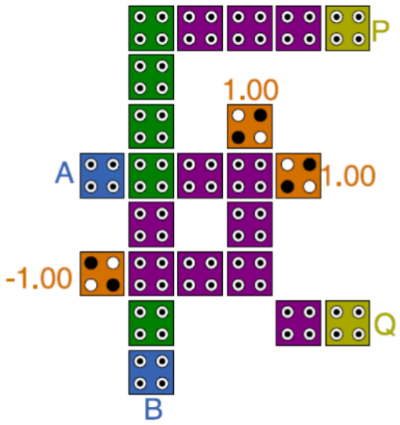


FIGURE 1(B) -Feynman Gate-2018

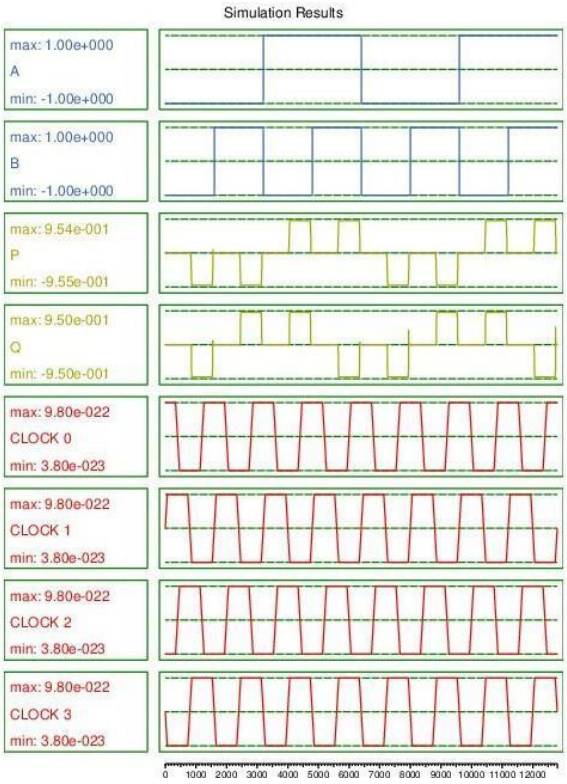


FIGURE1(B) - Feynman Gate Simulation-2019

C) Proposed CNOT Gate:

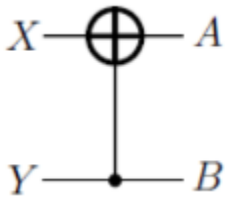


FIGURE 1(C) - Circuit representation of CNOT gate

From the circuit representation of the CNOT gate, X and Y are inputs, and A and B are

the outputs of the circuit. The logical equation of the outputs is represented as

A = X^Y

B = Y

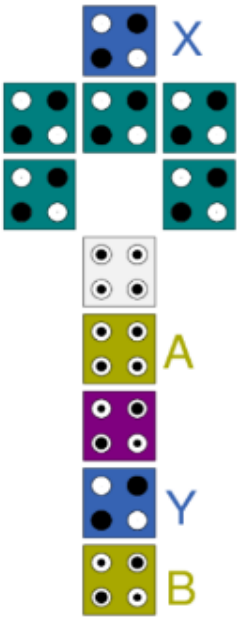


FIGURE 1(C) - proposed CNOT Gate

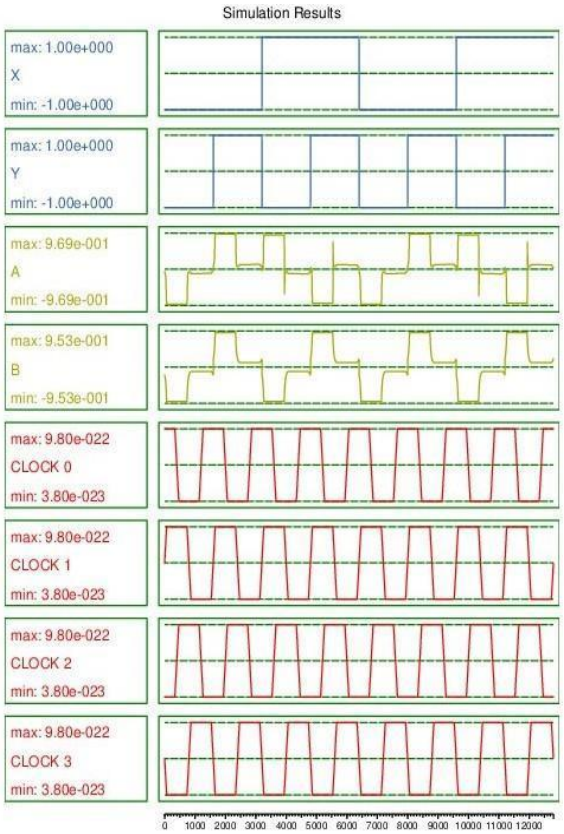


FIGURE 1(C) - proposed CNOT Gate Simulation

Comparison:

CNOT Gate	Cell count	Cell area (nm2)	Delay	MV gates	Wire crossover
1(A)	58	15660	1.5	4	coplanar
1(B)	23	7452	0.5	2	Not required
1(C)	11	3564	0	0	None

Majority voter(MV) gates cause a delay in the circuit. The Delay of the proposed circuit is zero. It is due to zero mv gates and doesn't carry any garbage values in the Output. From the graph, There is no delay between

the rising edge of the input to the corresponding output that is negligible.

2] DOUBLE CNOT GATE

The QCA layout standards, which require that all input cells should arrive in the same time zone, are followed by all of the recommended designs. Long QCA wires should be separated into numerous clock zones while taking into account the maximum number of cells and the minimum number of cells in the same zone to minimize excessive signal propagation and switching delays. There are no crossover options in any of the proposed designs.

Truth Table:

Two input and 2 output

X	Y	A	B
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

TABLE 2: Double CNOT Gate 2 INPUTS

Three inputs and three outputs

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

TABLE 3: Double CNOT Gate 3 INPUTS

A) Double Feynman gate - 2017

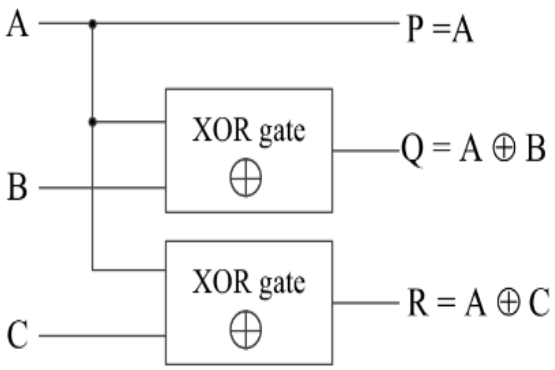


FIGURE 2(A) - Circuit representation of Double CNOT gate-2017

9A, B and C are inputs of the circuit and P, Q and R ate outputs. The logical equation of the outputs of figure 2(A) Circuit representation is

P = A

Q = A ^ B

R = A ^ C

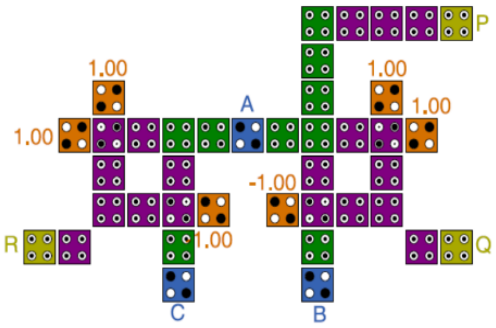


FIGURE 2(A)- Double CNOT Gate-2017

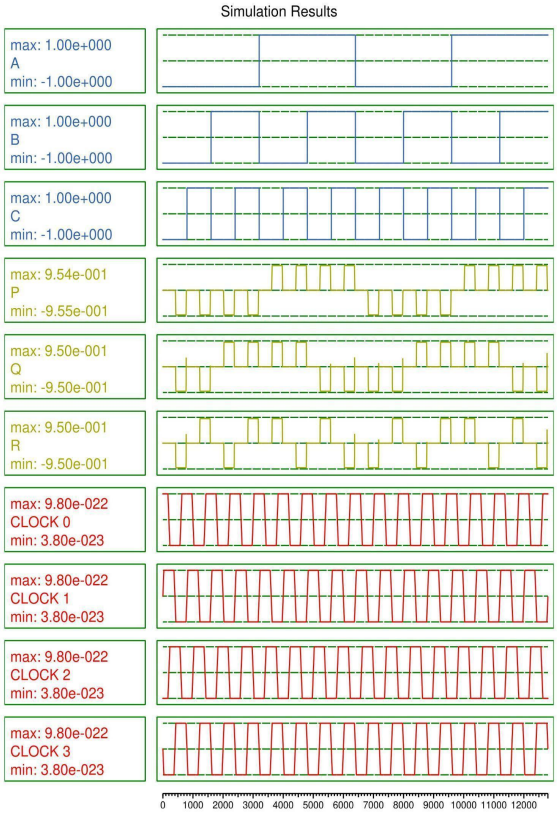


FIGURE 2(A) -Double Feynman Simulation-2017

B) Proposed Double CNOT Gate:

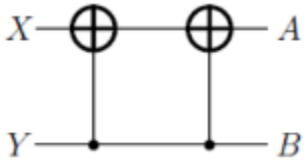


FIGURE 2(B) - Circuit representation of Double CNOT gate

X and Y are inputs of the circuit and A and B are the outputs. The logical equation of the outputs of figure 1(C) Circuit representation is

A = (X^Y)^Y

B = Y

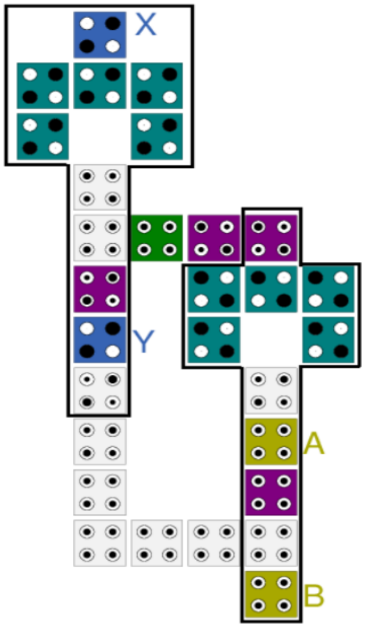


FIGURE 2(B) - Proposed Double CNOT Gate

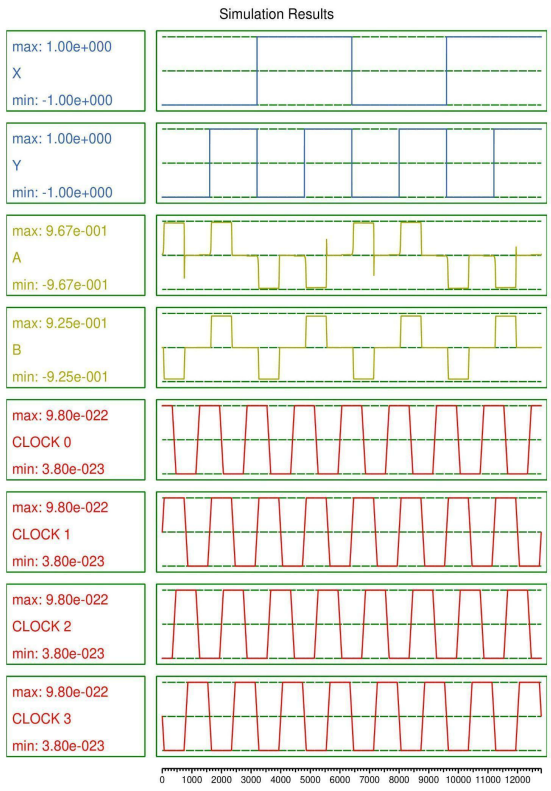


FIGURE 2(B) - Proposed Double CNOT Gate Simulation

Comparison:

DOUBLE CNOT Gate	Cell count	Cell area (nm2)	Delay	MV gates	Wire crossover
2(B)	29	9396	2	0	None
2(A)	40	12960	4	4	Coplanar

3] TOFFOLI GATE

A universal reversible gate, or TOFFOLI gate was proposed by Tommaso Toffoli and can be used to create the reversible analogue of any classical gate. It is also known as the "controlled-controlled-not" gate. It inverts the third bit if the first and second bits are 1.

Truth Table:

X	Y	Z	A	B	C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	0	1	1

TABLE 3: TOFFOLI GATE

A) TOFFOLI GATE - 2019

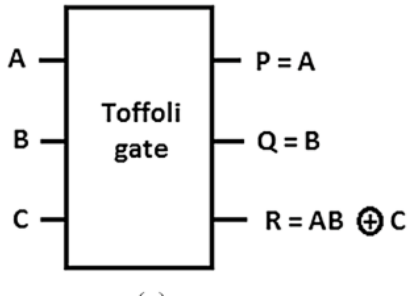


FIGURE 3(A) - Circuit representation of TOFFOLI gate-2019

A, B and C are inputs of the circuit and P, Q and R ate outputs. The logical equation of the outputs of figure 2(A) Circuit representation is

P = A
Q = B
R = (A . B) ^ C

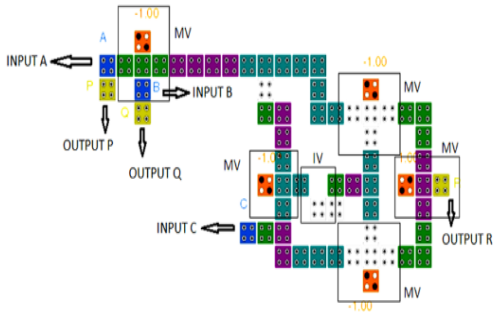


FIGURE 3(A) - TOFFOLI gate-2019

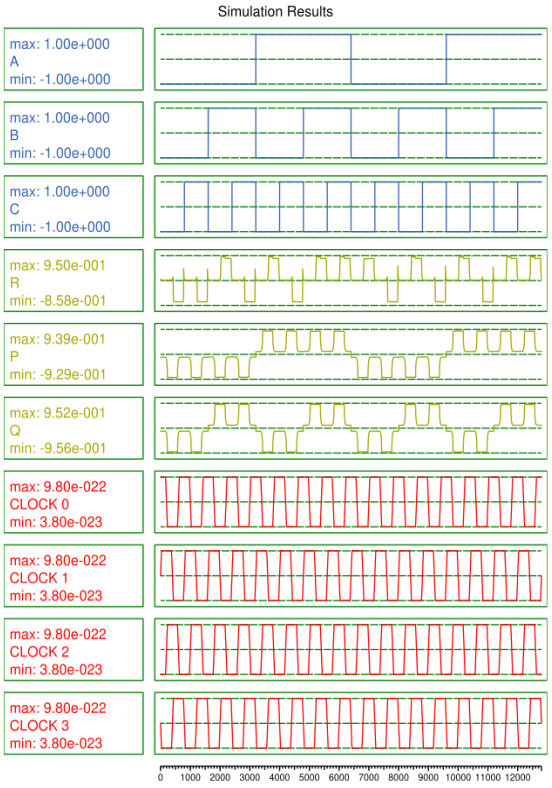


FIGURE 3(A) - Simulation

B) TOFFOLI GATE - 2017

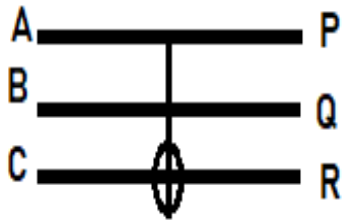


FIGURE 3(B) - Circuit representation of TOFFOLI gate

A, B and C are inputs of the circuit and P, Q and R ate outputs. The logical equation of the outputs of figure 2(A) Circuit representation is

P = A

Q = B

R = (A . B) ^ C

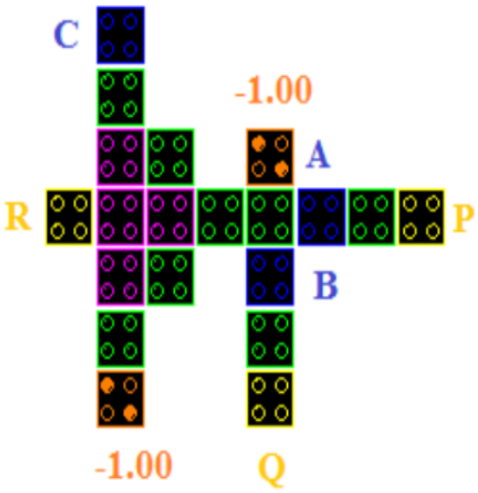


FIGURE 3(B).TOFFOLI Gate-2017

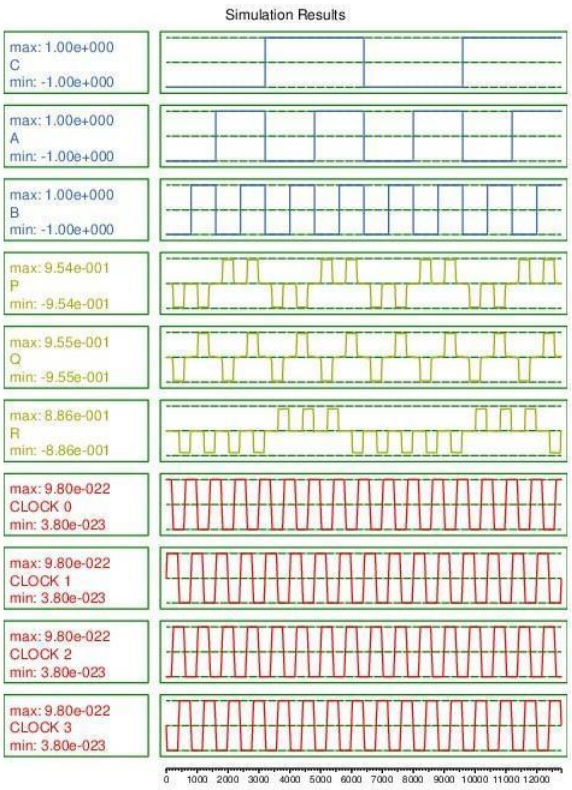


FIGURE 3(B) TOFFOLI Gate-2017- Simulation

C) Proposed TOFFOLI gate:

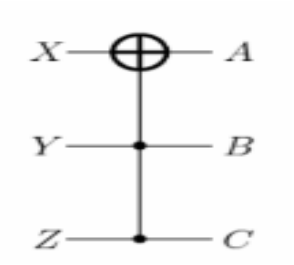


FIGURE 3(C) - Circuit representation of TOFFOLI gate

X, Y, and Z are the inputs and A, B, and C outputs. The logical equation of the outputs of figure 3(C) Circuit representation is

A = X^ (Y.Z)

B = Y

C = Z

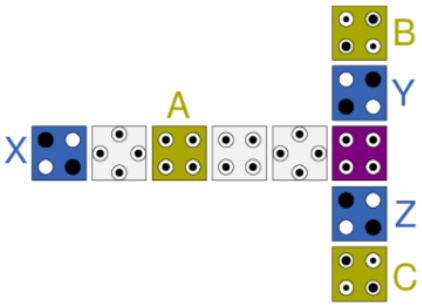


FIGURE 3(C) - proposed Toffoli Gate

In the proposed TOFFOLI Gate X, Y and Z are the Inputs of the circuits. There is the direct Transfer of the data from outputs A, B and C respectively.

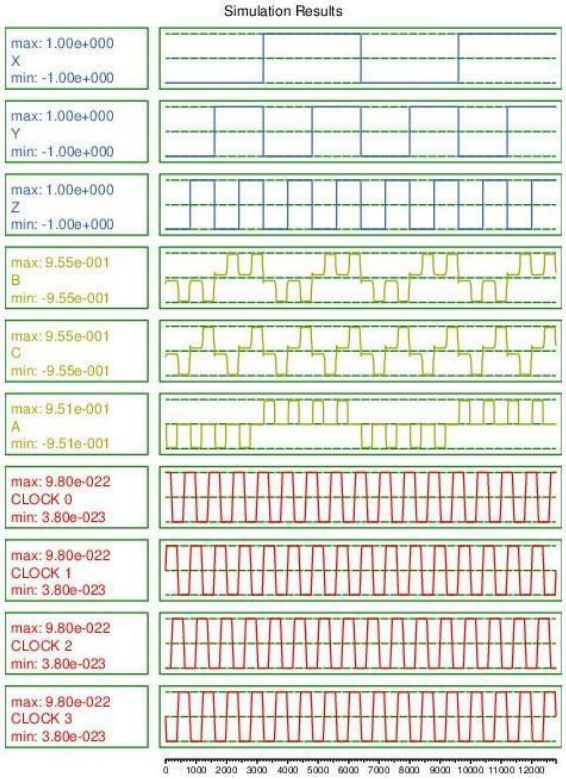


FIGURE 3(C) -proposed Toffoli Gate simulation

Comparison:

TOFFOLI Gate	Cell count	Cell area (nm2)	Delay	MV gates	Wire crossover
3(A)	64	20736	1.5	5	Coplanar
3(B)	34	11016	0.75	3	Multilayer

3(C)	10	3240	1	0	None

4] DOUBLE TOFFOLI GATE

Truth Table:

X	Y	Z	A	B	C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

TABLE 4: DOUBLE TOFFOLI GATE

A) Proposed DOUBLE TOFFOLI gate

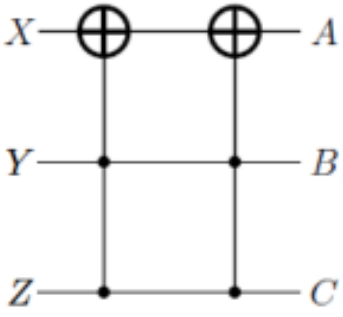


FIGURE 4(A) - Circuit representation of DOUBLE TOFFOLI gate

X, Y, Z are the inputs and A, B, C outputs. The logical equation of the outputs of figure 4(A) Circuit representation is

A = (X^(Y.Z))^(Y.Z)

B =Y

C = Z

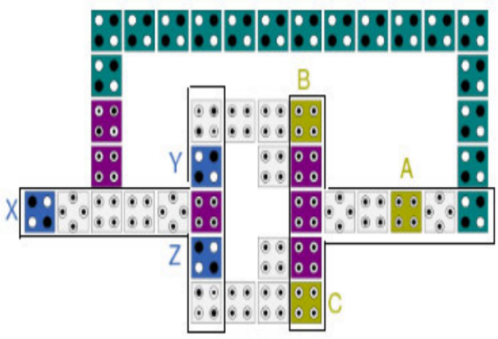


FIGURE 4(A)-proposed Double TOFFOLI Gate

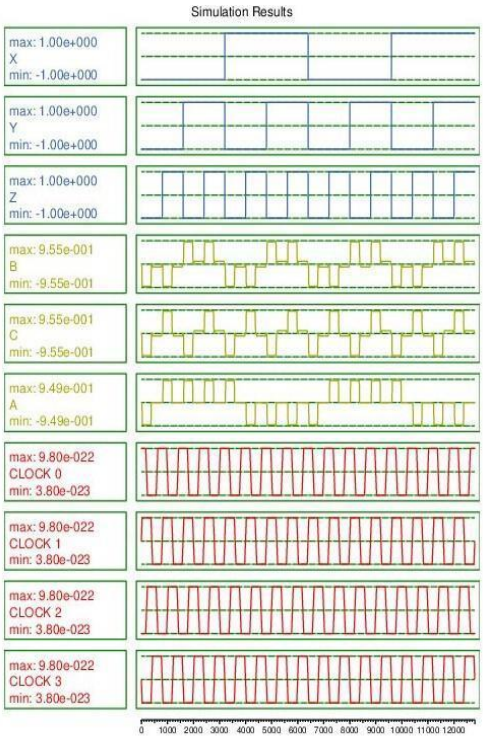


FIGURE 4(A)-proposed Double TOFFOLI GateSimulation

5]SINGLE TOFFOLI WITH 5 NOT GATES

Truth Table:

X	Y	A	B
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

TABLE 5: SINGLE TOFFOLI GATE AND 5 NOT GATES

A) Proposed SINGLE TOFFOLI GATE AND 5 NOT GATES

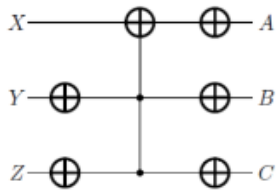


FIGURE 5(A) - Circuit representation of SINGLE TOFFOLI GATE AND 5 NOT GATES

X, Y, Z are the inputs and A, B, C outputs. The logical equation of the outputs of figure 5(A) Circuit representation is

A = [~(X^(~Y . ~Z))]

B = Y

C = Z

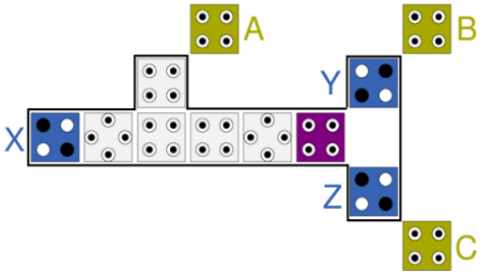


FIGURE 5(A)-proposed SINGLE TOFFOLI GATE AND 5 NOT GATES

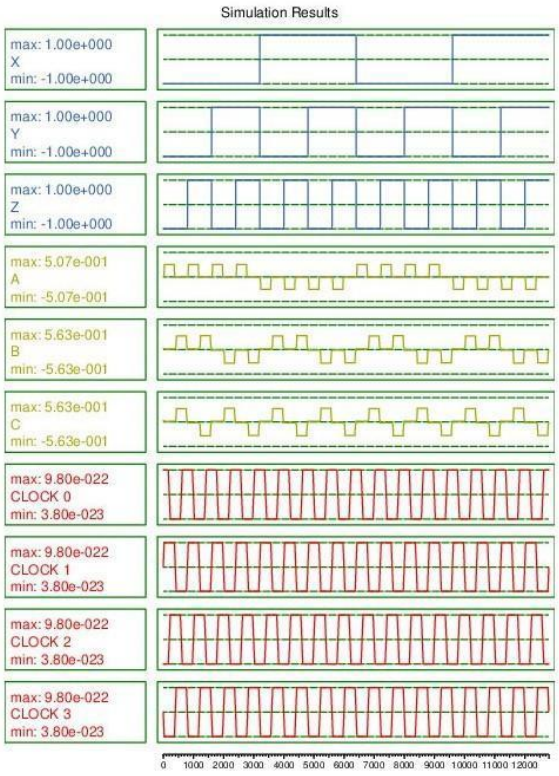


FIGURE-5(A)-SINGLE TOFFOLI GATE AND 5 NOT GATES Simulation

6) SWAP CIRCUIT

The inputs of the swap circuits are swapped and shown as the outputs in this circuit.

Truth Table:

X	Y	A	B
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

TABLE 6: SWAP CIRCUIT

A)SWAP Circuit 2017

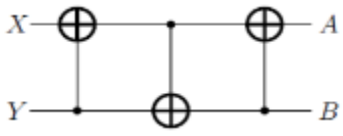


FIGURE 6(A) - Circuit representation of SWAP Circuit

X and Y are inputs of the circuit and A and B are the outputs. The logical equation of the outputs of figure 6(A) Circuit representation is

A =(X^Y)^(Y^(X^Y))

B = Y^(X^Y)

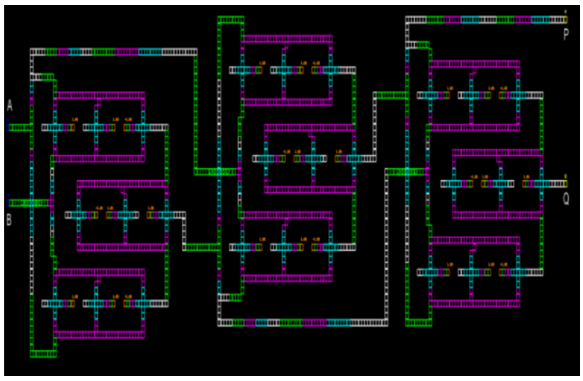


FIGURE 6(A)-SWAP Circuit-2017

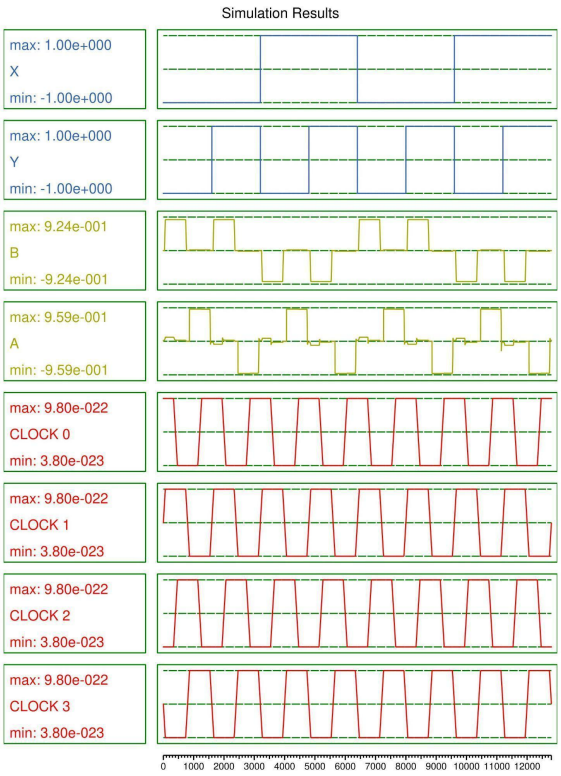


FIGURE 6(A)-Swap Circuit Simulation-2017

B) proposed SWAP circuit

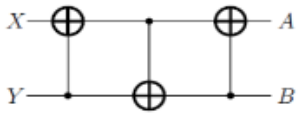


FIGURE 6(B) - Circuit representation of SWAP Circuit

X and Y are inputs of the circuit and A and B are the outputs. The logical equation of the outputs of figure 6(A) Circuit representation is

A =(X^Y)^(Y^(X^Y))

B = Y^(X^Y)

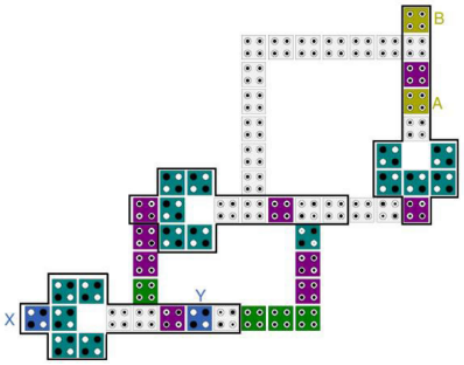


FIGURE 6(B)-proposed SWAP Circuit

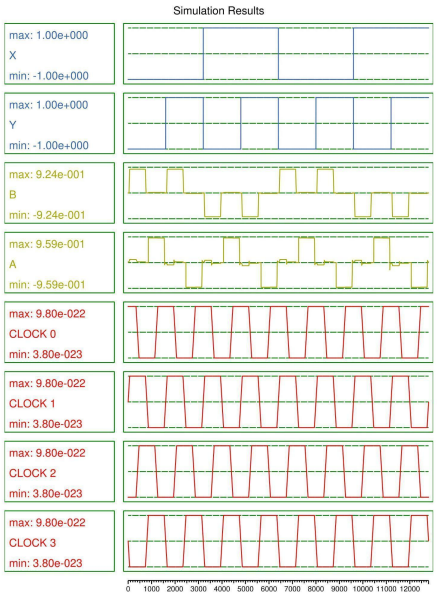


FIGURE 6(B)-Swap Circuit Simulation

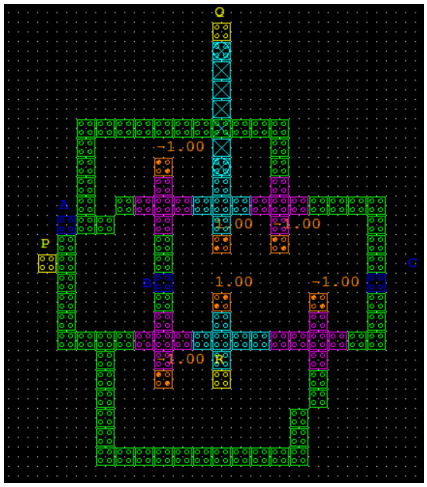
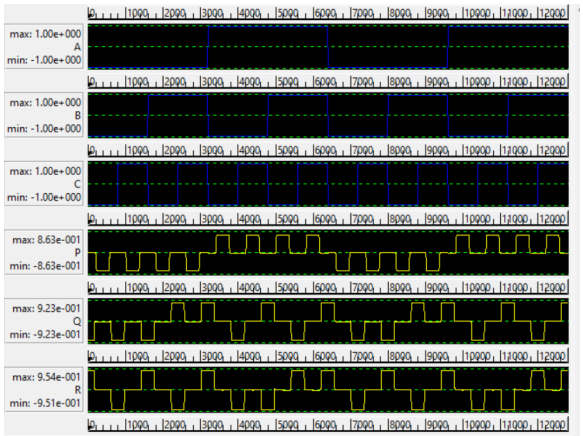


FIGURE 6(c)-Swap_circuit_using Fredkin2 Simulation



Comparison:

SWAP Circuit	Cell count	Cell area (nm2)	Delay	MV gates	Wire crossover
6(A)	135	43750	2.75	0	Multilayer
6(B)	55	17820	2	0	None

Logically and Physically Reversible Design Methodology

In QCA circuits, energy dissipation is primarily attributed to the irreversible nature of the majority gate, which has three inputs and a single output [32]. This irreversibility leads to information loss and consequent energy wastage in the environment. Figure (7a) represents the logical design (schematic) of the conventional irreversible majority gate, illustrating its functionality. Figure (7b), on the other hand, presents the physical design (layout) of this gate, revealing how it is implemented on the QCA chip.Efforts to address the energy dissipation challenge in QCA circuits focus on the development of logically and physically reversible design methodologies, aiming to enhance energy efficiency while preserving information integrity.

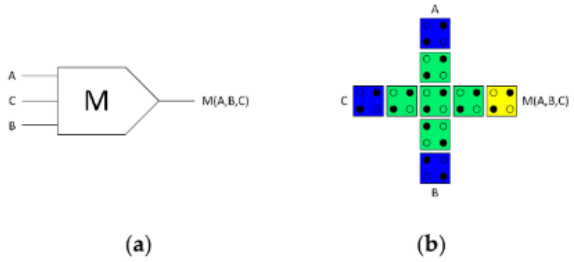


Figure 7.(a) Logical synthesis of the standard irreversible majority gate, Figure 7.(b) physical layout of the standard irreversible QCA majority gate.

To create a highly energy-efficient QCA Arithmetic Logic Unit (ALU), we introduced a pivotal innovation: a fully reversible majority gate. This gate, central to our design, duplicates input data, yielding an equal number of binary inputs and outputs. Figure 8 showcases this groundbreaking fully reversible majority gate, equipped with three inputs and three outputs due to data replication. This design strategy averts data loss and, crucially, safeguards against energy dissipation into the environment. Figure (8a) portrays the logical design (schematic), while Figure (8b) exhibits the physical layout (layout) of our fully reversible QCA majority gate.

Our study adopts a two-stage design approach, featured in Figure 9, to craft logically and physically reversible QCA ALU components. At the heart of this methodology lies the fully reversible majority gate, as detailed in Figure 8, which serves as the foundational building block. This approach marks a significant stride towards achieving enhanced energy efficiency and information integrity in quantum-dot cellular automata.

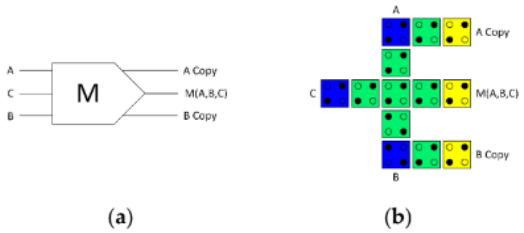


Figure 8. (a) Logical synthesis of the reversible majority gate; Figure 8.(b) physical layout of the reversible QCA majority gate

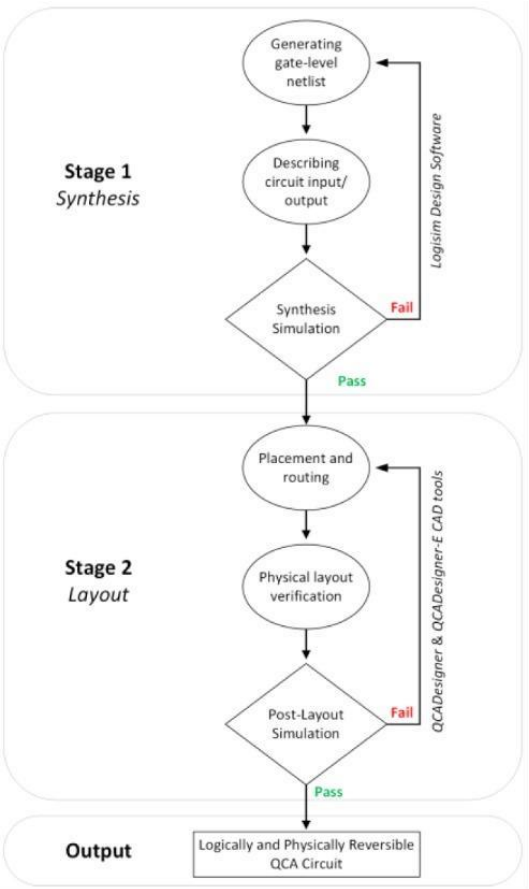


Figure 9. The methodology of designing

Logically and physically reversible QCA circuits..

Table 1. The employed technology and simulation parameters.

Parameter	Description	Value
QD size	Quantum-dot size	5 nm
Cell area	Dimensions of each cell	18 × 18 nm
Cell distance	Distance between two cells	2 nm
Layer separation	Distance between QCA layers in multilayer crossing	11.5 nm
Clock high	Max. saturation energy of clock signal	9.8×10^{-22} J
Clock low	Min. saturation energy of clock signal	3.8×10^{-23} J
Relative permittivity	Relative permittivity of material for QCA system (GaAs & AlGaAs)	12.9
Radius of effect	Maximum distance between cells whose interaction is considered	80 nm
Temp	Operating temperature	1 K
τ	Relaxation time	1×10^{-15} s
T_γ	Period of the clock signal	1×10^{-9} s
T_{in}	Period of the input signals	1×10^{-9} s
T_{step}	Time interval of each iteration step	1×10^{-16} s
T_{sim}	Total simulation time	8×10^{-9} s
γ_{shape}	Shape of clock signal slopes	GAUSSIAN
γ_{slope}	Rise and fall time of the clock signal slopes	1×10^{-10} s

1. Proposed Logically and Physically Reversible QCA ALU Design

The ALU, a pivotal component of the CPU, executes logical and arithmetic operations on incoming data, providing results to other registers, memory, or devices. Our study introduces a fully logically and physically reversible QCA ALU designed for ultralow-energy efficiency. It leverages a combination of logic circuits crafted around the fully reversible QCA majority gate from Figure 8.

The development process commenced with the creation of a high-level block diagram, as depicted in Figure 10. This reversible ALU architecture comprises three key components: the Logic Unit (LU), the Arithmetic Unit (AU), and the Control Unit (CU). The LU handles logical operations like AND, NAND, OR, NOR, XOR, XNOR, NOT, and data transfer. The AU tackles arithmetic operations, including addition, subtraction, multiplication, and division of binary numbers. The CU, guided by input S0, determines the operation type, be it arithmetic or logical.

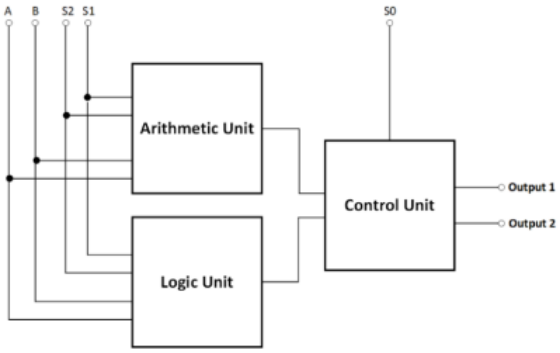
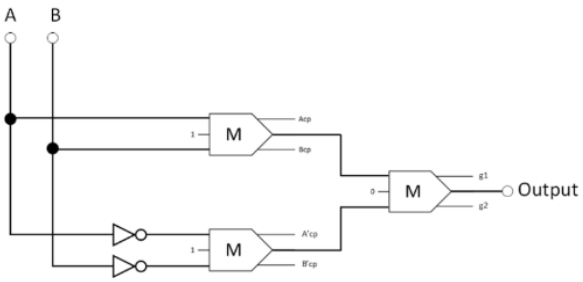


Figure 10. The High-level block diagram of the proposed reversible QCA ALU.

The reversible QCA ALU circuit takes two input operands, A and B, and generates two output values, Output1 and Output2. This reversibility allows the ALU to execute two arithmetic or two logical operations simultaneously, offering a total of 16 operations, encompassing eight logical and eight arithmetic operations, as detailed in Table 2. To specify the ALU's operation and operand selection, three input pins—S0, S1, and S3—are employed.

Table 2. The operations of the proposed reversible QCA ALU.

.



$$\text{Output} = (A + B)\cdot(\overline{A} + \overline{B}),$$

Figure 11. The synthesis of the proposed reversible XOR (Acp, Bcp, A'cp, and B'cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

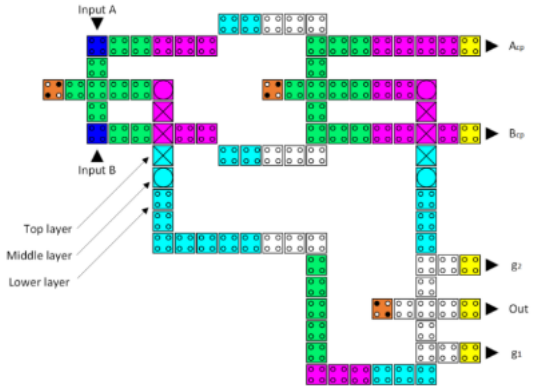


Figure 11(a). The layout of the proposed reversible QCA XOR (Acp and Bcp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

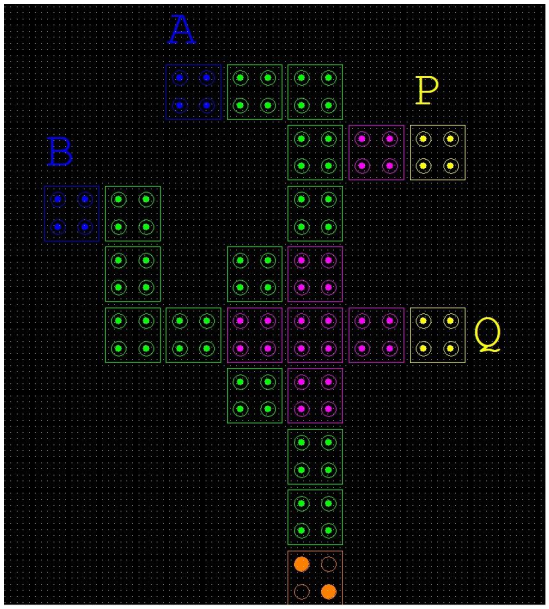


Figure 11(b). The layout of the proposed reversible QCA XOR Gate

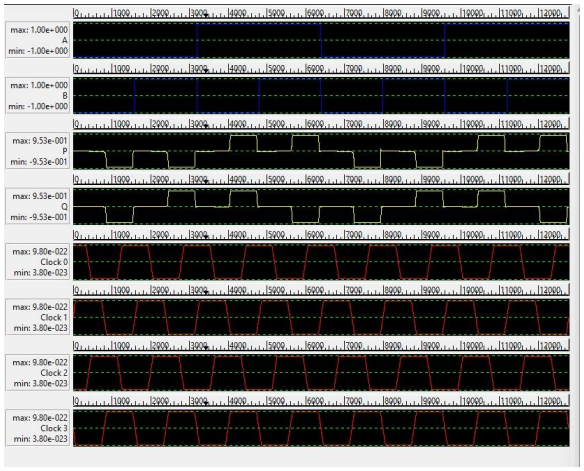


Figure 11(b). Output of the proposed XOR Gate.

A 2:1 multiplexer (mux) selects one of two input signals and passes it to the output based on a control signal. It acts as a data switch, allowing one of the inputs to be transmitted to the output line.

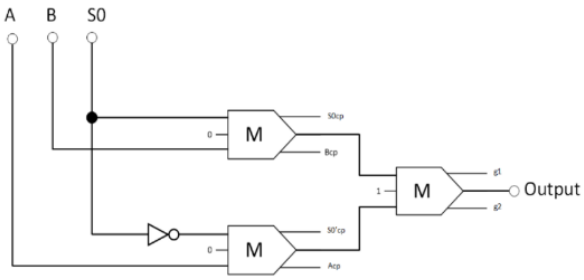


Figure 12. The synthesis of the proposed reversible 2:1 multiplexer (Acp, Bcp, S0cp, and S0′cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs.)

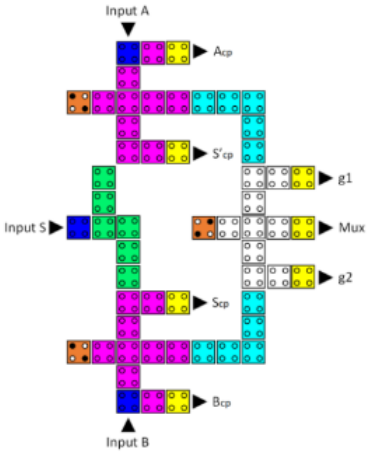


Figure 12(a). The layout of the proposed reversible QCA 2-to-1 multiplexer (Acp, Bcp, Scp, and S'cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

A 4:1 multiplexer (mux) takes four input signals and, based on a control signal, chooses one of those inputs to send to the output. It acts as a data selector, enabling the selection of one input from a set of four.

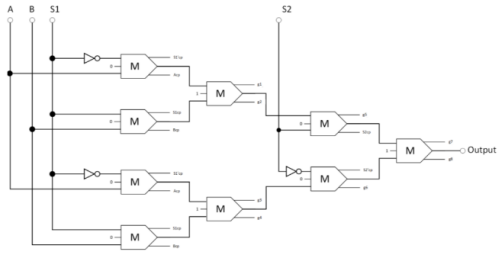


Figure 13.The synthesis of the proposed reversible 4:1 multiplexer (Acp, Bcp, S1cp, S2cp, S10cp, and S20cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs)

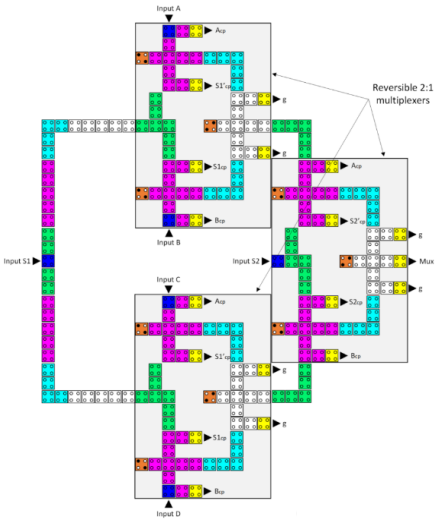


Figure 13(a) The layout of the proposed reversible QCA 4-to-1 multiplexer (Acp, Bcp, Ccp, Dcp,S1cp, S1'cp, S2cp, and S2'cp refer to copies of the input data, whereas g variables indicate the garbage outputs).

A reversible half-adder is a digital logic circuit that computes the sum and carries outputs for two binary inputs while maintaining reversibility, meaning it can accurately recover the original inputs from the outputs.

$$\text{Sum} = (A \cdot \overline{B}) + (\overline{A} \cdot B)$$
$$\text{Carry} = (A \cdot B),$$

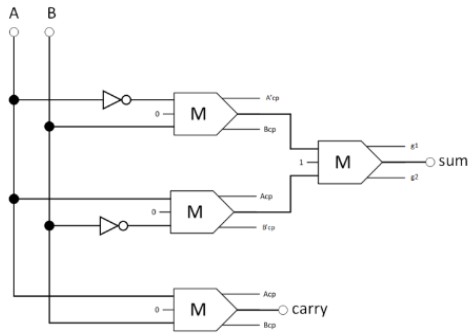


Figure 14. The synthesis of the proposed reversible half-adder (Acp, Bcp, A'cp, and B'cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

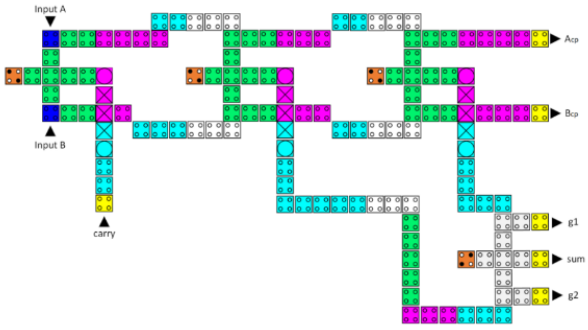


Figure 14(a). The layout of the proposed reversible QCA half-adder (Acp and Bcp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

A reversible half-subtractor is a digital logic circuit that computes the difference and borrows outputs for two binary inputs while remaining reversible, allowing the original inputs to be recovered from the outputs.

$$\text{Diff} = (\overline{A} \cdot B) + (A \cdot \overline{B})$$
$$\text{Borrow} = (\overline{A} \cdot B),$$

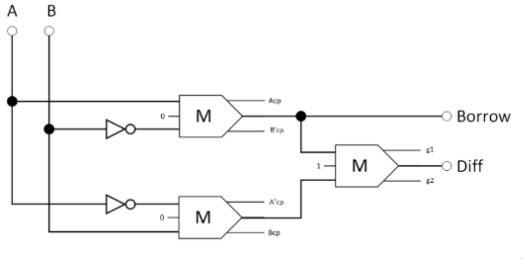


Figure 15. The synthesis of the proposed reversible half-subtractor (Acp, Bcp, A'cp, and B'cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

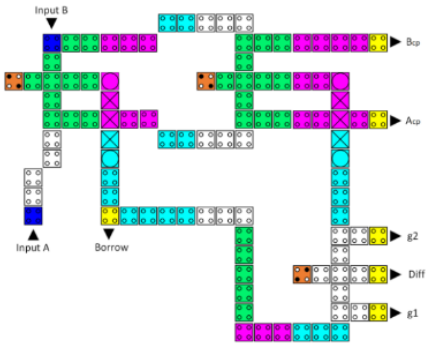


Figure 15(a). The layout of the proposed reversible QCA half-subtractor (Acp and Bcp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

Reversible Circuit (Logical Unit):

A reversible QCA LU (Logic Unit) is a component in quantum-dot cellular automata that performs logical operations while maintaining reversibility. It can compute operations like AND, OR, XOR, and more, and it ensures that the original inputs can be accurately retrieved from the outputs.

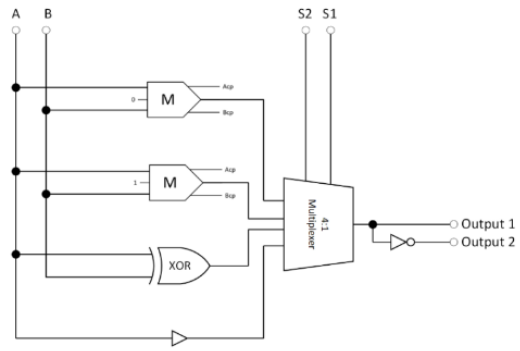


Figure 16. The synthesis of the proposed reversible LU (Acp and Bcp refer to copies of the inputs).

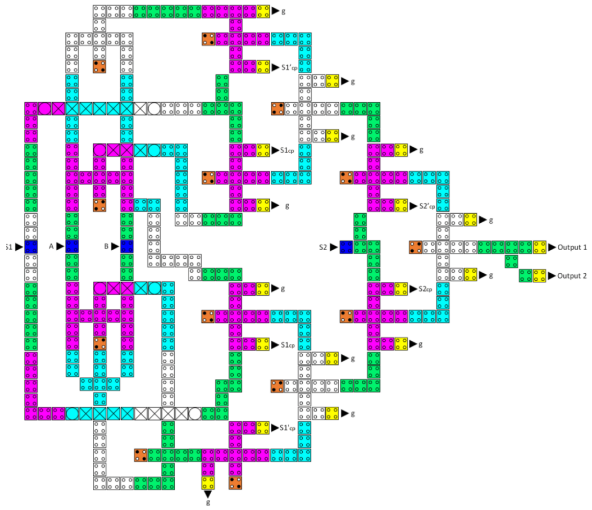


Figure 16(a). The layout of the proposed reversible QCA LU (S1cp, S1'cp, S2cp, and S2'cp refer to copies of the input data, whereas g variables indicate the garbage outputs).

Reversible Circuit (AU):

A reversible QCA AU (Arithmetic Unit) in Quantum-dot Cellular Automata handles arithmetic operations like addition, subtraction, multiplication, and division while preserving reversibility, allowing the original inputs to be recovered from the outputs.

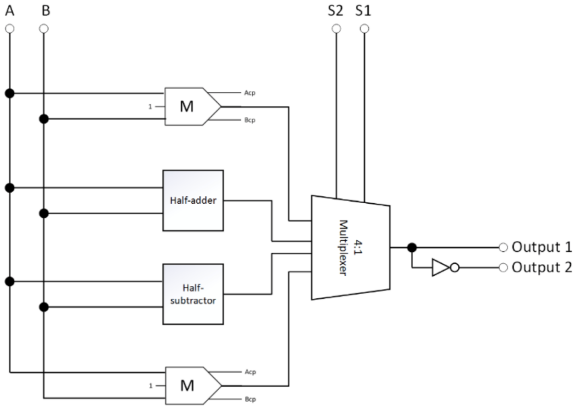


Figure 17. The synthesis of the proposed reversible AU (Acp and Bcp refer to copies of the inputs).

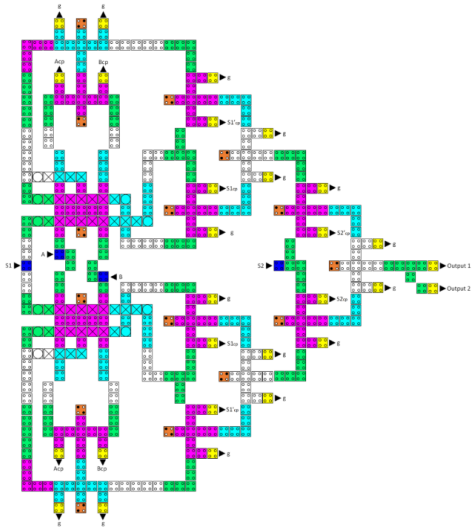


Figure 17(a). The layout of the proposed reversible QCA AU (Acp, Bcp, S1cp, S1'cp, S2cp, and S2'cp refer to copies of the input data, whereas g variables indicate the garbage outputs).

Reversible Circuit (ALU):

A reversible ALU is a digital circuit that performs arithmetic and logical operations while ensuring that the original input data

can be perfectly reconstructed from the outputs. It's designed for energy efficiency and is crucial in low-power computing systems like Quantum-dot Cellular Automata (QCA).

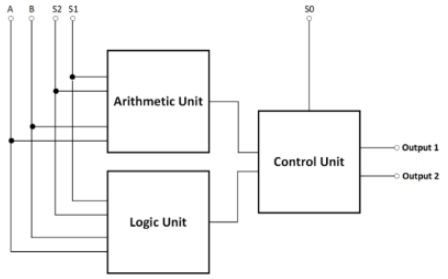


Figure 10. The High-level block diagram of the proposed reversible QCA ALU.

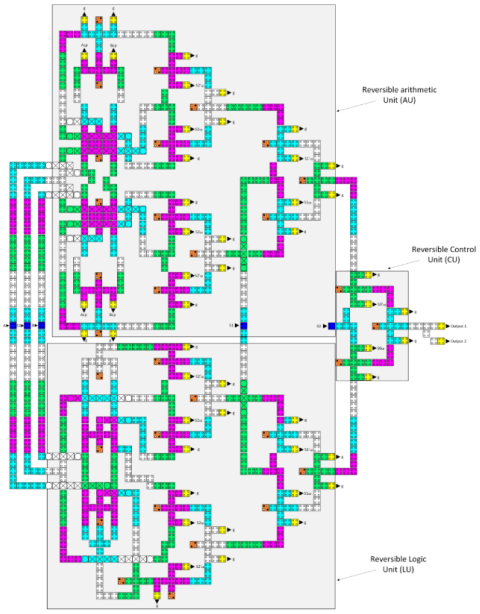


Figure 10(a). The layout of the proposed reversible QCA ALU (Acp, Bcp, Ccp, Dcp, S1cp, S1'cp, S1cp, S1'cp,S2cp, and S2'cp refer to copies of the input data, whereas g variables indicate the garbage outputs).

Conclusions :

In conclusion, this research has tackled a critical challenge in electronic devices: heat dissipation, through the innovative application of reversible QCA circuits. By introducing advanced gate designs like the CNOT and TOFFOLI gates, the study has not only reduced cell counts significantly but also enhanced energy efficiency. The introduction of a logically and physically reversible QCA ALU represents a major breakthrough, achieving exceptional energy efficiency and, critically, zero information loss. Through meticulous simulations, the study demonstrates minimal energy loss across the proposed designs. The proposed QCA ALU outperforms existing designs by a substantial 88.8% improvement in energy efficiency, accompanied by a marked reduction in cell count and physical footprint. As a prospect for the future, this research can pave the way for further advancements, including the extension of these concepts to accommodate additional operations and the development of energy-efficient multi-bit ALU circuits. The emerging experimental work in QCA technology, particularly using silicon-based quantum dots, holds immense potential for practical nanoscience applications and for advancing the field.

References:

1. Design and Analysis of a Novel Low-Power Exclusive-OR Gate Based on Quantum-Dot Cellular Automata (Research paper)
2. Nanomaterials-13-02445 (Research Paper)
3. Wikipedia,youtube

Contribution:

Group Lead: **Alkesh Shukla (S20210020252)**

I have Implemented the Toffoli Gate 2017, Proposed Double Toffoli Gate, Proposed Double Toffoli Gate and 5 NoT Gate, Proposed CNOT Gate, Reversible 2:1 MUX, CNOT Gate 2018, Reversible Half Adder, Reversible LU and Reversible AU.

Anish Kamble (S20210020253)

I have implemented Toffoli Gate 2019, Swap Circuit,Proposed Toffoli Gate, Proposed Double CNOT Gate, Reversible Half Subtractor, CNOT Gate 2019, Reversible 4:1 MUX, Reversible ALU, Reversible XOR Gate.

Implemented Noval Circuit Circuit:

We're teaming up to create a super-efficient Reversible Circuit. Our latest achievements include a Reversible XOR gate using a Majority Gate and a swap circuit using the Fredkin gate. These innovations are not only highly effective but also take up fewer cells.